TITLE OF THE INVENTION

Path Searcher for Spread Spectrum Receiver

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to spread spectrum (CDMA) communication systems and more specifically to a path searcher for use in a spread spectrum receiver for detecting delay characteristics of a plurality of communication paths for a diversity demodulator such as RAKE demodulator by taking correlation between a replica of a scrambled synchronization code and a received spread spectrum signal.

Description of the Related Art

Diversity combining is a well known technique in the art of spread spectrum systems to achieve gain of a received signal by combining component signals of different communication paths. This is achieved by the knowledge of individual path delays. In order to determine the individual path delays, a scrambled synchronization code is transmitted as a timing message. At the receiving site, the sync code is detected by taking correlation between the received signal and a replica of the scrambled sync code. Correlation values of the individual communication paths represent their delay characteristics. Since the correlation values must be obtained on a chip-by-chip basis, the amount of computations is significant and places a heavy burden on hardware. For example, if the scrambled sync code has "P" symbols and the number of chips per symbol is "S", and correlation is taken at "T" points, multiplying and summing operations must be performed "P x S x T" times for detecting a sync code.

In a prior art base station receiver of spread spectrum communication network, the correlation technique requires the use of T correlators for each mobile user, with a total number of m x T correlators for each base station.

A technique is known to reduce this number by storing a P x T chip length of a received spread spectrum signal in a memory and repeatedly reading the stored data for correlation. However, a high capacity memory is required to hold this amount of information.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a path searcher for a spread spectrum receiver which requires a smaller number of correlators.

According to a first aspect of the present invention, there is provided a path searcher for a spread spectrum receiver for receiving a spread spectrum signal containing a scrambled synchronization code, wherein the receiver includes a plurality of correlators and each correlator produces a replica of the scrambled synchronization code and determines a correlation value between the replica and the received spread spectrum signal. The present invention is characterized in that each of the correlators performs a correlation operation between the received spread spectrum signal and the replica at a rate higher than a chip rate of the spread spectrum signal by successively shifting the replica with respect to the spread spectrum signal.

According to a second aspect, the present invention provides a path searcher for a spread spectrum receiver for receiving a spread spectrum signal, wherein the receiver includes a plurality of correlators, and each of the correlators produces a replica of a scrambled synchronization code and

determines a correlation value between the replica and the received spread spectrum signal. The invention is characterized by a first memory for storing the received spread spectrum signal. Each of the correlators reads the stored spread spectrum signal from the first memory at a rate higher than a chip rate of the received spread spectrum signal, repeatedly performs a correlation operation between the read spread spectrum signal and the replica at the higher rate by successively shifting the replica with respect to the stored spread spectrum signal. A second memory is provided for initially storing an intermediate result of a correlation value from each of the correlators and subsequently reading the stored intermediate result into a corresponding one of the correlators. Each of the correlators adds the intermediate result from the second memory with a correlation value produced by the correlation operation performed at the end of the chip interval.

BRIEF DESCRIPTION OF THE DRAWIGNS

The present invention will be described in detail further with reference to the following drawings, in which:

Fig. 1 is a block diagram of a spread spectrum receiver incorporating a path searcher of the present invention;

Fig. 2 is a block diagram of the path searcher according to a first embodiment of the present invention;

Fig. 3 is a block diagram of the multiplier of Fig. 2;

Fig. 4 is an illustration of results of multiplications of Fig. 3;

Fig. 5 is a timing diagram of the path searcher of Fig. 2;

Fig. 6 is a block diagram of the adder of Fig. 2 and the associated memory;

Fig. 7 is a block diagram of the path searcher according to a second embodiment of the present invention;

Fig. 8 is a block diagram of the multiplier of Fig. 7; and

Fig. 9 is an illustration of results of multiplications of Fig. 8;

Fig. 10 is a timing diagram of the path searcher of Fig. 7; and

Fig. 11 is a block diagram of the adder of Fig. 8 and the associated circuits.

DETAILED DESCRIPTION

Referring to Fig. 1, a spread spectrum receiver according to the present invention is comprised of N antenna systems or diversity branches each including an antenna 1 for receiving a spread spectrum signal propagated over a multipath fading channel, an RF receiver or down-converter 2 for down-converting the received signal, an A/D converter 3 for converting the down-converted signal to digital form, and a band-pass filter 4 for limiting the frequencies of the digital signal to a predetermined bandwidth.

For purposes of disclosure, it is assumed that the spread spectrum receiver of the present invention is located in a base station of a mobile communication system. Mobile stations are each assigned a unique scramble code which is multiplied by a channelization code to produce a spreading code. The spreading code is used to scramble the information-bearing signal of a mobile station and transmitted on a forward channel to the base station. A synchronization code is scrambled with the spreading code and transmitted on the forward channel to allow the base station to establish synchronization.

The outputs of the N diversity branches are supplied to a path

searcher 5 and a demodulator 6. Path searcher 5 produces correlation values of multiple communication paths from the transmitter to the respective antennas 1 in a manner as will be described later. Demodulator 6 has a number of RAKE fingers corresponding to the diversity branches to demodulate their output signals by using the correlation values. A decoder 7 provides an error correction and decoding process on the demodulated signal.

As shown in Fig. 2, the path searcher 5 of a first embodiment of the present invention includes a plurality of identical correlators 10-1 ~ 10-m, which are provided in number corresponding to the number of mobile users. If correlation values are determined at "T" points for each of "m" users, the number of correlators 10 is given by T x m/Q, where Q is the number of times by which each correlator must repeat correlation operations between scrambled signals. If the chip rate of the spread spectrum signal is 3.84 MHz and the operating speed of the correlators is 61.44 MHz, the integer "Q" is equal to 16. If T = Q, the number of correlators 10 is equal to the number of mobile users. Otherwise, the number of correlators 10 increases depending on the number T of correlation points. As long as the integer T is not much greater than the integer Q, the number of correlators required to produce sufficient amount of delay information is significantly smaller than what is required in the prior art. It will be seen that by increasing the calculation speed of the correlators with respect to the chip rate of the spread spectrum signal, the number of correlators can be decreased.

A plurality of PN (pseudonoise) generators 11-1 ~ 11-m are provided for m users' scrambling codes. A controller 12 provides overall timing and

selecting functions of the correlators.

Each correlator 10 is comprised of a selector 14 that uses a control signal from the controller 12 to select one of the scrambling codes corresponding to a user and supplies a replica generator 15 with the selected scrambling code. Replica generator 15 includes a mapping table 15A in which synchronization codes are mapped to channelization codes. One of the channelization codes and the corresponding sync code are selected from the mapping table 15A by the controller 12 corresponding to a received spread spectrum signal. The selected channelization code is supplied to a multiplier circuit 15B, where it is multiplied by the scrambling code from the selected PN generator to produce a spreading code which is identical to that used by the mobile user. Since the received spread spectrum signal contains a scrambled sync code, the spreading code used in the forward channel is reproduced in this way. The reproduced spreading code is then used by the spreading circuit 15C for scrambling the selected sync code to produce a replica of the transmitted scrambled sync code.

The output signals of the band-pass filters 4 are applied to a selector 16 and one of these is selected by the controller 12 and supplied to a multiplier 17. In the multiplier 17 a correlation operation is repeatedly performed between the replica and the output signal of the selected band-pass filter 4 at a rate higher than the chip rate of the received spread spectrum signal.

As shown in detail in Fig. 3, the multiplier 17 includes shift registers 41 and 42. If the scrambled sync code has 2,560 chips and the number (T) of correlation points is 16, the shift register 41 has 2,560 stages for loading the scrambled sync code from the spreading circuit 15C and is driven at the chip

rate 3.84 MHz for shifting and recirculating the stored chips through a recirculating path 44. Shift register 42 has T x Q (256 = 16 x 16) stages which are divided into sixteen sets of sixteen stages Q0 to Q15 and all Q0 to Q15 stages of each set are connected to the R0 to R15 stages of shift register, respectively. These register stages are also designated T0 to T15 stages since they correspond to the T = 16 correlation points. Shift register 42 receives chip data from the T0 to T15 stages at the chip rate 3.84 in response to a load pulse applied thereto. As a result, each of sixteen chips on stages T0 to T15 of shift register 41 are copied as same sixteen chips on the Q0 to Q15 stages of shift register 42, with a total of 256 chips. In response to a shift pulse, the shift register 42 is driven at 61. 44 MHz which is sixteen times higher than the chip rate for shifting and circulating the replicated chips through a recirculating path 45.

A plurality of multiplier units 43-1 to 43-16 are provided. First input terminals of these multiplier units 43 are connected to the sixteen Q0 stages of register 42 and their second input terminals are connected together to the output of selector 16 to receive a spread spectrum signal. For convenience, the spread spectrum signal is represented as a sequence of signal chips S0, S1, ..., S2559. Each of these signal chips is applied to the multiplier units 43 for a match (or multiplication) with chips moving on the shift register 41. Therefore, for each signal chip, multiplication is repeatedly performed Q = 16 times during a chip interval with a resolution of T = 16 points on the replica's chip sequence.

While 256 chips of the replica are moving along the stages of register 42 at the rate of 61.44 MHz, the output signal of the selector 16 is supplied

one chip at a time for a match with these chips to produce a plurality of multiplication values from the multiplier units 43-1 through 43-16.

The following is a description of one example of the multiplication process of Fig. 3 with reference to Fig. 4 by assuming that a sequence of signal chips S0 to S15 is supplied to the multiplier units 43 when replica chips #1 through #2,560 chips are stored in stages R0 through R2559, respectively. It is seen that the signal chip S0 is simultaneously multiplied by replica chips #1 to #16 of the R0 to R15 stages by repeatedly multiplying their 16 copies at Q0 to Q15 stages of register 42, producing 256 multiplication values. When signal chip S1 is applied, the shift register 41 is shifted by one chip position to the left, causing chips #2 through #17 to be loaded into the register 42. Signal chip S1 is therefore multiplied by copies of these chips at Q0 to Q15 stages of register 42, producing 256 multiplication values. The process is repeated on subsequent signal chips, producing a total of 4,096 multiplication values during a period of signal chips S0 to S15, as shown in Fig. 5.

Returning to Fig. 2, the output signals of multiplier 17 are supplied to an adder 18 where the multiplication values are summed and supplied to a dual-port RAM 19 as intermediate results of a correlation value and stored therein an interval corresponding to each multiplication process and then read out of this memory as a previous value.

As shown in detail in Fig. 6, the adder 18 includes a plurality of adder units 18-1 through 18-16 to which the output signals of multiplier 17 are respectively supplied. A set of output values of these adder units, which correspond to correlation points T0 to T15, are stored in respective storage locations of the memory 19. When a subsequent set of multiplication values

are supplied to the adder units 18 from the multiplier 17, the memory is accessed to read its contents and feed them to the adder units so that the new multiplication values are summed with corresponding previous values in the adder units 18-1 through 18-16. The summed values are used to update the stored previous values of the memory 19. The process is repeated until multiply-and-add process is performed sixteen times for each chip interval, producing correlation values. The correlation values produced in this way from each correlator 10 are delivered through an output gate 20 to the demodulator 6.

Demodulator uses the correlation values as delay characteristics of the communication paths to control its RAKE fingers in a manner known in the art.

It is seen from the foregoing that the present invention obtains high definition path delay data with the use of a small number of correlators.

Since the dual-port RAM 19 must be accessed each time a multiply-and-add process is performed, a wide bandwidth is required for accessing this memory. It is desirable that the bandwidth of a memory be as narrow as possible by reducing the number of repeated accesses.

A second embodiment of the present invention shown in Fig. 7 satisfies this need. In this modification, two dual-port RAMs 31 and 32 are provided respectively on the input and output sides of all correlators 10-1 ~ 10-m, as common storage areas. Read-write operations of these memories are controlled by the controller 12.

The output signals of all band-pass filters 4 are supplied to the input RAM 31 and stored in this memory for sixteen consecutive chip intervals.

The stored signals are read out of this memory to the selector 16, and one of these signals is selected and coupled to a multiplier 21 of each correlator.

As shown in detail in Fig. 8, the multiplier 21 is essentially similar to the multiplier 17 of Fig. 3. Multiplier 21 differs in that the shift register 41 is driven at 1/16 of the chip rate 3.84 MHz and the shift register 42 responds to a load pulse which occurs at the same 3.84/16 MHz rate and the stored chips are shifted at the chip rate 3.84 MHz. The sixteen signal chips of RAM 31 are supplied via the selector 16 and applied respectively to the multiplier units 43-1 ~ 43-16.

The operation of the multiplier of Fig. 8 will be understood with reference to Figs. 9 and 10 by assuming that signal chips S0 to S15 are supplied to the multiplier units 43-1 ~ 43-16 respectively when replica chips #1 through #2,560 chips are stored in stages R0 through R2559. Signal chips S0 to S15 are respectively multiplied by replica chips #1 to #16 of the R0 to R15 stages by multiplying their 16 copies at all the Q0 stages of register 42 during a first chip interval, producing 256 multiplication values. During a second chip interval, the shift register 42 is shifted by one chip position to the left, causing the copies of replica chips # 2 to #17 to be shifted from the Q1 stages to the Q0 stages. Signal chips S0 to S14 are therefore multiplied by copies of these chips at the Q0 stages of register 42, producing 256 multiplication values. The process is repeated during subsequent chip interval until the chips S0 to S15 are multiplied respectively by #16 to #31 chips which have been shifted from the Q15 stages to the Q0 stages during the sixteenth chip interval, producing a total of 4,096 multiplication values during the sixteen chip intervals, as shown in Fig. 10.

As shown in detail in Fig. 11, the adder 22 includes a plurality of adder units 22-1 through 22-16 to which the output signals of multiplier 21 are respectively supplied. Output signals of these adder units, which correspond to correlation points T0 to T15, are stored in respective storage locations of a delay memory or flip-flop 23 for an interval corresponding to a multiplying operation. When a subsequent set of new multiplication values are supplied to the adder units 22 from the multiplier 21, the flip-flop 23 supplies the stored values to a selector 24. Selector 24 passes these signals to the adder 22 as previous values, where they are summed with the new values from the multiplier 21. The summed outputs are fed to the flip-flop 23 to update the previous values. The outputs of flip-flop 23 are also supplied to the output RAM 32 and stored in respective storage locations by overwriting previous values. The process continues until the multiplications are repeated fifteen times, so that a total value of the previous fifteen values is stored in a storage location of memory 32 corresponding to each of the correlation points T0 to T15. At the end of sixteenth calculation, the selector 24 switches its paths and the memory 32 is accessed to read the intermediate results of the previous calculations. The outputs of the memory 32 are passed through the switched paths of selector 24 to the adders 22, respectively, where the intermediate results are summed with the final results to produce sixteen correlation values at the outputs of the flip-flop 23.

An output gate 33 is enabled to pass the correlation values obtained in this way to the demodulator 6.